In the Claims:

Please cancel Claims 1, 3, 11, 13, 14, 16, 19, 21, and 22.

Please amend the claims as follows:

2. (amended) The assembly according to Claim 15 wherein said unpackaged semiconductor device is an integrated circuit chip having an active and a passive surface, said first coupling members attached to said active surface.

4. (amended) The assembly according to Claim 15 further comprising at least one passive electrical component integrated into said conductive lines on said interconnector.

5. (amended) The assembly according to Claim 15 wherein said entry ports are spaced apart less than 100 μm center to center, and said exit ports are spaced apart more than 100 μm center to center.

6. (amended) The assembly according to Claim 15 wherein said interconnector is a flexible polyimide film.

7. (amended) The assembly according to Claim 15 wherein said electrically conductive lines are made of a material selected from a group consisting of copper, copper alloy, or copper plated with tin, tin alloy, silver, or gold.

8. (amended) The assembly according to Claim 15 wherein said first and second coupling members are solder balls selected from a group consisting of pure tin, tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

9. (amended) The assembly according to Claim 15 wherein said first coupling members are selected from a group consisting of gold bumps, copper bumps, copper/nickel/palladium bumps, and z-axis conductive epoxy.

10. (amended) The assembly according to Claim 15 further having an adhesive non-conductive polymer underfilling any spaces between said first coupling members attached to said entry ports under said semiconductor device.

12. (amended) The assembly according to Claim 15 further comprising at least one discreet passive electrical component attached to said ports.

15. (amended) A semiconductor assembly comprising:

a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

said interconnector having on said first surface electrically conductive lines for connecting a plurality of packaged semiconductor devices formed on said first surface adjacent to each other;

said interconnect further having electrically conductive paths extending through said interconnector from said first surface to said second surface, forming electrical ports on said second surface;

said ports comprise first and second pluralities, said first plurality ports spaced apart by less, center to center, than said second plurality ports are spaced apart, center to center;

said interconnector folded so that said adjacent semiconductor devices are stacked on top of each other;

at least one additional unpackaged semiconductor device having a plurality of first electrical coupling members, said first coupling members attached to said first plurality ports; and

a plurality of second electrical coupling members attached to said second plurality ports, said coupling members suitable for attachment to other parts.

17. (amended) The method according to Claim 23 further comprising the step of:

integrating at least one passive electrical component into said conductive lines on said interconnector.

18. (amended) The method according to Claim 23 further comprising the step of:

underfilling an adhesive non-conductive polymer into any spaces between said first coupling members attached to said entry ports under said semiconductor device.

20. (amended) The method according to Claim 23 further comprising the step of:

attaching at least one discreet passive electrical component to said ports.

23. (amended) A method of assembling an integrated circuit device, comprising the steps of:

forming electrically conductive lines on a strip-like flexible interconnector of electrically insulating material having first and second surfaces;

forming electrically conductive paths extending through said interconnector from said first surface to said second surface, forming electrical ports on said second surface such that said ports comprise first and second pluralities, said first plurality ports spaced apart less, center to center, than said second plurality ports are spaced apart, center to center;

forming on said first surface a plurality of packaged semiconductor devices adjacent to each other and connected to said conductive lines;

attaching at least one additional unpackaged semiconductor device, having a plurality of first electrical coupling members, to said first plurality ports;

attaching a plurality of second electrical coupling members to said second plurality ports; and